19-1523; Rev 4, 7/01

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

General Description

The 1.25Gbps MAX3264/MAX3268 and the 2.5Gbps MAX3265/MAX3269/MAX3765 limiting amplifiers are designed for Gigabit Ethernet and Fibre Channel optical receiver systems. The amplifiers accept a wide range of input voltages and provide constant-level output voltages with controlled edge speeds. Additional features include RMS power detectors with programmable loss-of-signal (LOS) indication, an optional squelch function that mutes the data output signal when the input voltage falls below a programmable threshold, and excellent jitter performance.

The MAX3264/MAX3265/MAX3765 feature current-mode logic (CML) data outputs that are tolerant of inductive connectors and a 16-pin TSSOP package, making these circuits ideal for GBIC receivers. The MAX3268/MAX3269 feature standards-compliant positive-referenced emitter-coupled logic (PECL) data outputs and are available in a tiny 10-pin µMAX package that is ideal for small-form-factor receivers.

Applications

Gigabit Ethernet Optical Receivers

Fibre Channel Optical Receivers

System Interconnect

ATM Optical Receivers

Selector Guide appears at end of data sheet.
Pin Configurations appear at end of data sheet.

Features

- **+3.0V to +5.5V Supply Voltage**
- **Low Deterministic Jitter**
  14ps (MAX3264)
  11ps (MAX3265/MAX3765)
- **150ps (max) Edge Speed (MAX3265/MAX3765)**
  300ps (max) Edge Speed (MAX3264)
- **Programmable Signal-Detect Function**
- **Choice of CML or PECL Output Interface**
- **10-Pin µMAX or 16-Pin TSSOP Package**

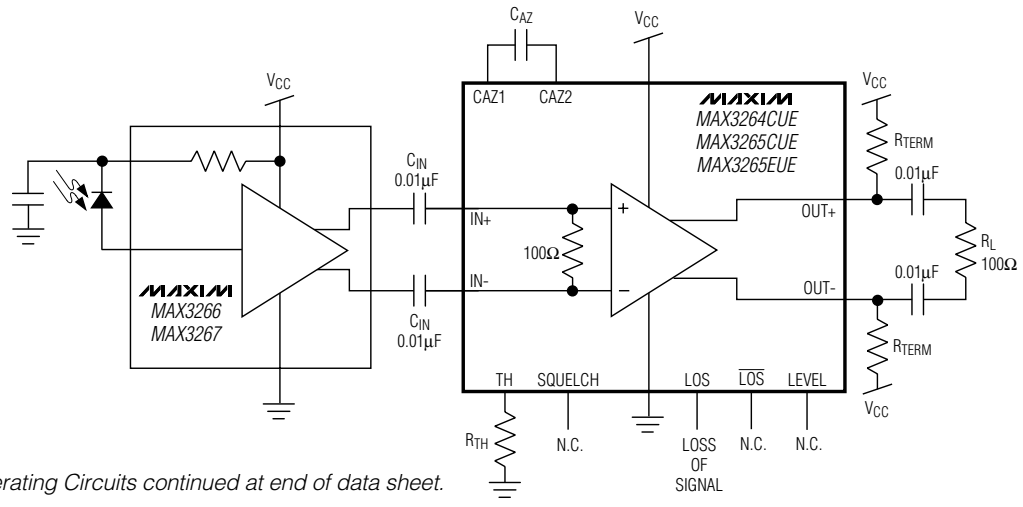
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3264CUE	0°C to +70°C	16 TSSOP-EP†
MAX3264C/D	0°C to +70°C	Dice*
MAX3265CUE	0°C to +70°C	16 TSSOP-EP†
MAX3265CUB	0°C to +70°C	10 µMAX-EP†
MAX3265C/D	0°C to +70°C	Dice*
MAX3265EUE	-40°C to +85°C	16 TSSOP-EP†
MAX3268CUB	0°C to +70°C	10 µMAX-EP†
MAX3268C/D	0°C to +70°C	Dice*
MAX3269CUB	0°C to +70°C	10 µMAX-EP†
MAX3269C/D	0°C to +70°C	Dice*
MAX3765CUB	0°C to +70°C	10 µMAX-EP†

**Dice are designed to operate from 0°C to +70°C, but are tested and guaranteed only at T_A = +25°C.*

†EP = Exposed paddle

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....-0.5V to +6.0V
Voltage at IN+, IN- .....(V_{CC} - 2.4V) to (V_{CC} + 0.5V)
Voltage at SQUELCH, CAZ1, CAZ2, LOS, $\overline{LOS}$, TH.....-0.5V to (V_{CC} + 0.5V)
Voltage at LEVEL.....-0.5V to +2.0V
Current into LOS, $\overline{LOS}$ .....-1mA to +9mA
Differential Input Voltage (IN+ - IN-) 2.5V
Continuous Current at CML Outputs (OUT+, OUT-).....-25mA to +25mA
Continuous Current at PECL Outputs (OUT+, OUT-) 50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 27mW/°C above +70°C) 2162mW
10-Pin µMAX (derate 20mW/°C above +70°C).....1600mW
Operating Ambient Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Processing Temperature (dice) .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Data outputs terminated per Figure 1, V_{CC} = +3.0V to +5.5V, **T_A = 0°C to +70°C**. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Data Rate	MAX3264/MAX3268			1.25		Gbps
	MAX3265/MAX3269/MAX3765			2.5		
Input Voltage Range	MAX3264/MAX3268		5		1200	mV
	MAX3265/MAX3269/MAX3765		10		1200	
Deterministic Jitter	MAX3264/MAX3268 (Notes 2, 3)			14	30	psp-p
	MAX3265/MAX3269/MAX3765 (Notes 2, 3)			11	25	
Random Jitter	MAX3264/MAX3268 (Notes 2, 4)			15		ps_{RMS}
	MAX3265/MAX3269/MAX3765 (Notes 2, 4)			8		
Data Output Edge Speed	MAX3264 (Note 5)		80	175	300	ps
	MAX3265/MAX3765 (Note 6)			100	150	
	MAX3268 (Note 5)		80	150	300	
	MAX3269 (Note 6)			100	150	
LOS Hysteresis	(Notes 2, 7)		2.5	4.4		dB
LOS Assert/Deassert Time	(Notes 7, 8)			1		µs
Low LOS Assert Level	R_{TH} = 2.5kΩ	MAX3264/MAX3268	1.20	2.6		mV
		MAX3265/MAX3269/MAX3765	2.20	4.8		
Low LOS Deassert Level	R_{TH} = 2.5kΩ	MAX3264/MAX3268		4.5		mV
		MAX3265/MAX3269/MAX3765		8.5		

ELECTRICAL CHARACTERISTICS (continued)

(Data outputs terminated per Figure 1, V_{CC} = +3.0V to +5.5V, **T_A = 0°C to +70°C**. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Medium LOS Assert Level	R_{TH} = 7kΩ	MAX3264/MAX3268		5.6	9		mV
		MAX3265/MAX3269/MAX3765		9.9	16		
Medium LOS Deassert Level	R_{TH} = 7kΩ	MAX3264/MAX3268			15	19.8	mV
		MAX3265/MAX3269/MAX3765			27	40.5	
High LOS Assert Level	R_{TH} = 20kΩ	MAX3264/MAX3268		9.4	21.6		mV
		MAX3265/MAX3269/MAX3765		18.0	41.5		
High LOS Deassert Level	R_{TH} = 20kΩ	MAX3264/MAX3268			35		mV
		MAX3265/MAX3269/MAX3765			67		
Squelch Input Current				0	80	400	µA
Differential Input Resistance	IN+ to IN-			97	100	103	Ω
Input-Referred Noise	MAX3264/MAX3268				150		$µV_{RMS}$
	MAX3265/MAX3269/MAX3765				230		
CML Output Voltage	LEVEL = open, R_{LOAD} = 50Ω			550		1200	mV
	LEVEL = GND and R_{LOAD} = 75Ω			1100	1270	1800	
PECL Output High Voltage	Referenced to V_{CC}			-1.025		-0.880	V
PECL Output Low Voltage	Referenced to V_{CC}			-1.810		1.620	V
LOS Output High Voltage	I_{LOS} = -30µA			2.4			V
LOS Output Low Voltage	I_{LOS} = +1.2mA					0.4	V
Output Signal When Squelched	Outputs AC-coupled				20		mV
Power-Supply Rejection Ratio	f < 2MHz				20		dB
Low-Frequency Cutoff	C_{AZ} = open				2		MHz
	C_{AZ} = 0.1µF				2		kHz
Output Resistance (single ended)	MAX3264/MAX3265/MAX3765			85	100	115	Ω
	MAX3268/MAX3269				4		
Power-Supply Current	Figure 2		MAX3268		39	62	mA
			MAX3269		48	78	
		Output not squelched	MAX3264		38	62	
			MAX3265		50	76	
			MAX3765		50	76	
		Output squelched	MAX3765		64	90	

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

ELECTRICAL CHARACTERISTICS—MAX3265EUE

(Data outputs terminated per Figure 1, V_{CC} = +3.0V to +5.5V, **T_A = -40°C to +85°C**. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate			2.5		Gbps
Input Voltage Range		10		1200	mV
Deterministic Jitter	(Notes 2, 3)		11	25	ps_{p-p}
Random Jitter	(Notes 2, 4)		8		ps_{RMS}
Data Output Edge Speed	(Note 6)		100	155	ps
LOS Hysteresis	(Notes 2, 7)	2.2	4.4		dB
LOS Assert/Deassert Time	(Notes 7, 8)		1		µs
Low LOS Assert Level	R_{TH} = 2.5kΩ	2.20	4.8		mV
Low LOS Deassert Level	R_{TH} = 2.5kΩ		8.5	13.6	mV
Medium LOS Assert Level	R_{TH} = 7kΩ	9.9	16		mV
Medium LOS Deassert Level	R_{TH} = 7kΩ		27	43.0	mV
High LOS Assert Level	R_{TH} = 20kΩ	18.0	41.5		mV
High LOS Deassert Level	R_{TH} = 20kΩ		67	111	mV
Squelch Input Current		0	80	400	µA
Differential Input Resistance	IN+ to IN-	97	100	103	Ω
Input-Referred Noise			230		$µV_{RMS}$
CML Output Voltage	LEVEL = open, R_{LOAD} = 50Ω	550		1200	mV
	LEVEL = GND, R_{LOAD} = 75Ω	1100	1270	1800	
LOS Output High Voltage	I_{LOS} = -30µA	2.4			V
LOS Output Low Voltage	I_{LOS} = +1.2mA			0.450	V
Output Signal When Squelched	Outputs AC-coupled		20		mV
Power-Supply Rejection Ratio	f < 2MHz		20		dB
Low-Frequency Cutoff	C_{AZ} = open		2		MHz
	C_{AZ} = 0.1µF		2		kHz
Output Resistance (single ended)		85	100	115	Ω
Power-Supply Current	Figure 2		50	76	mA

Note 1: Specifications for Input Voltage Range, LOS Assert/Deassert Levels, and CML Output Voltage refer to the total differential peak-to-peak signal applied or measured. PECL output voltages are absolute (single-ended) voltages measured at a single output.

Note 2: Input edge speed is controlled using 4-pole, lowpass Bessel filters with bandwidth approximately 75% of the maximum data rate.

Note 3: Deterministic jitter is measured with a K28.5 pattern (0011 1110 1011 0000 0101). Deterministic jitter is the peak-to-peak deviation from ideal time crossings, measured at the zero-level crossings of the differential output per ANSI X3.230, Annex A.

Note 4: Random jitter is measured with the minimum input signal applied after filtering with a 4-pole, lowpass, Bessel filter (frequency bandwidth at 75% of the maximum data rate). For Fibre Channel and Gigabit Ethernet applications, the peak-to-peak random jitter is 14.1-times the RMS random jitter.

Note 5: Input signal applied after a 933MHz Bessel filter.

Note 6: Input signal applied after a 1.8GHz Bessel filter.

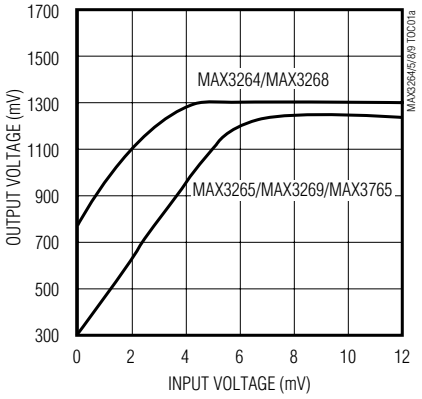
Note 7: Input for LOS assert/deassert and hysteresis tests is a repeating K28.5 pattern. Hysteresis is defined as: $20\log (V_{LOS\text{-}DEASSERT} / V_{LOS\text{-}ASSERT})$.

Note 8: Response time to a 10dB change in input power.

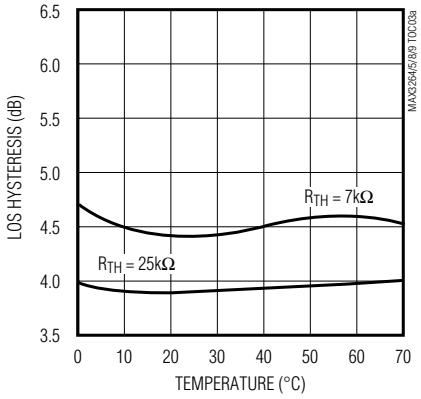
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

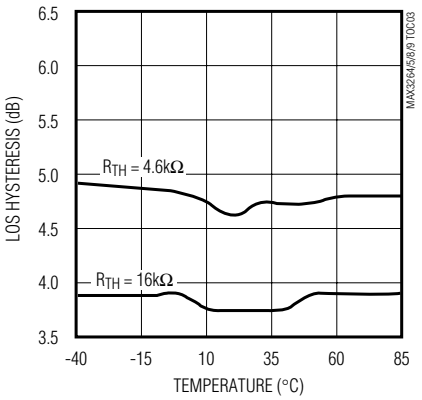
OUTPUT VOLTAGE vs. INPUT VOLTAGE



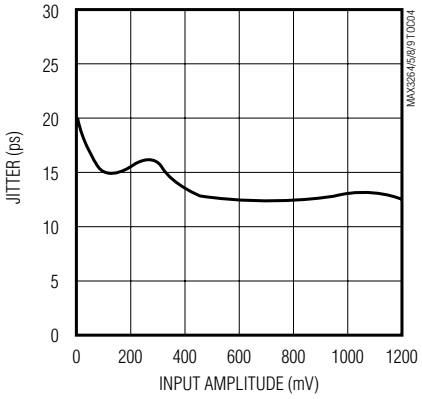
MAX3264 LOS HYSTERESIS vs. TEMPERATURE



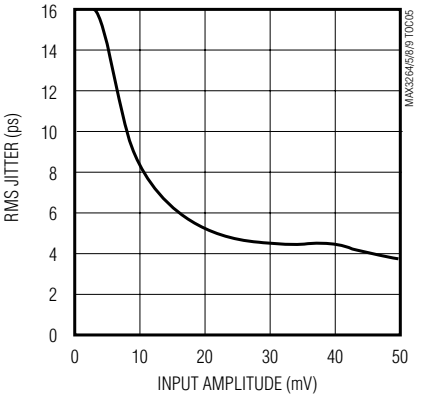
MAX3265EUE LOS HYSTERESIS vs. TEMPERATURE



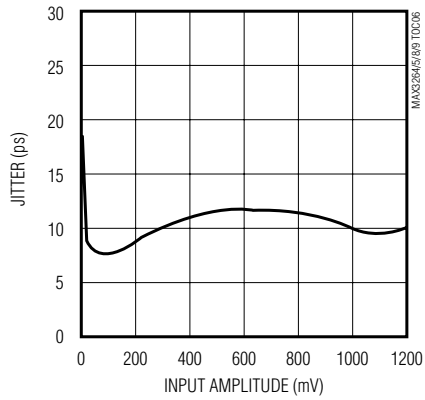
MAX3264/MAX3268 DETERMINISTIC JITTER vs. INPUT AMPLITUDE



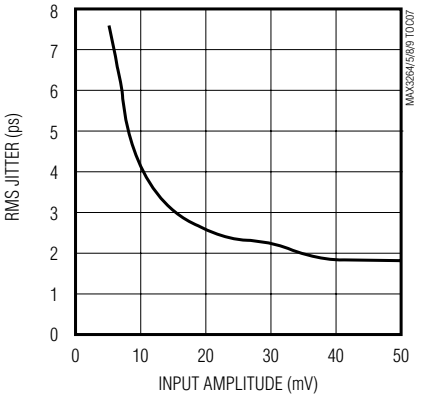
MAX3264/MAX3268 RANDOM JITTER vs. INPUT AMPLITUDE



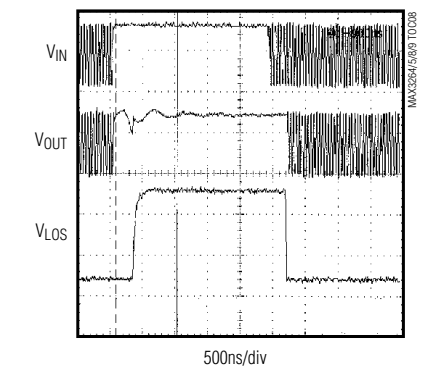
MAX3265/MAX3269/MAX3765 DETERMINISTIC JITTER vs. INPUT AMPLITUDE



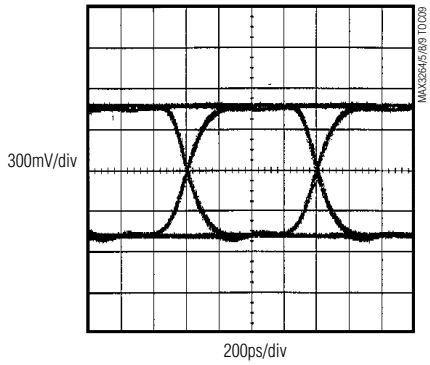
MAX3265/MAX3269/MAX3765 RANDOM JITTER vs. INPUT AMPLITUDE



LOSS OF SIGNAL WITH SQUELCH



MAX3268 DATA OUTPUT EYE DIAGRAM (MINIMUM INPUT)

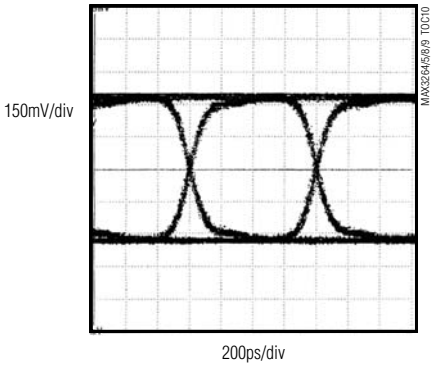


3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

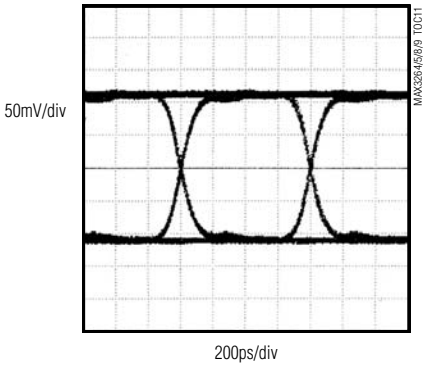
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

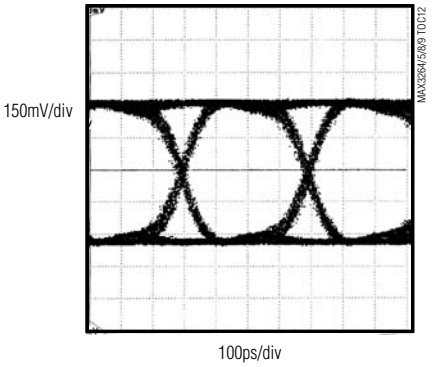
MAX3264 DATA OUTPUT EYE DIAGRAM AT 1.25Gbps (MINIMUM INPUT)



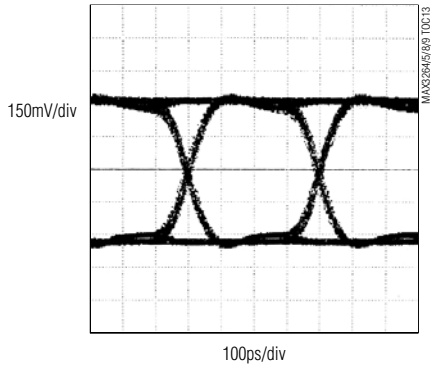
MAX3264 DATA OUTPUT EYE DIAGRAM AT 1.25Gbps (MAXIMUM INPUT)



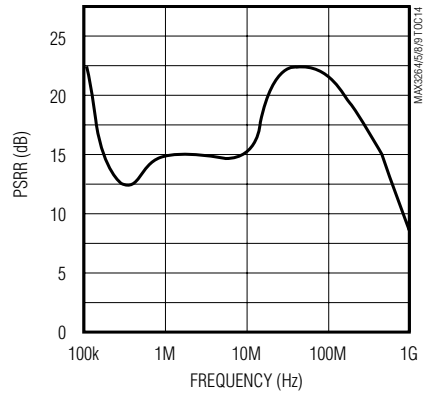
MAX3265/MAX3765 DATA OUTPUT EYE DIAGRAM 2.5Gbps (MINIMUM INPUT)



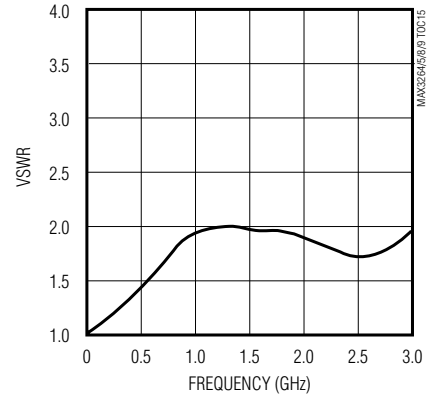
MAX3265/MAX3765 DATA OUTPUT EYE DIAGRAM 2.5Gbps (MAXIMUM INPUT)



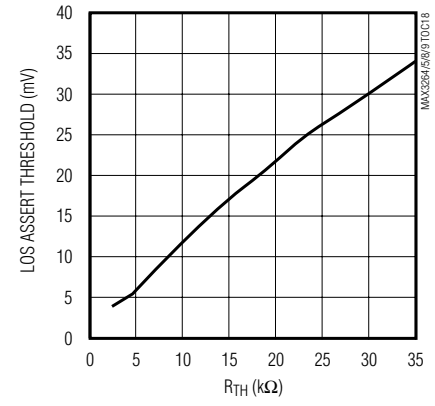
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



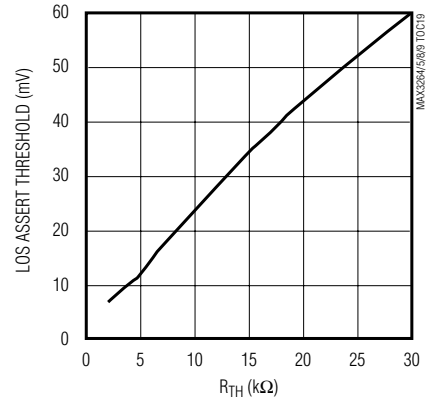
OUTPUT VSWR vs. FREQUENCY



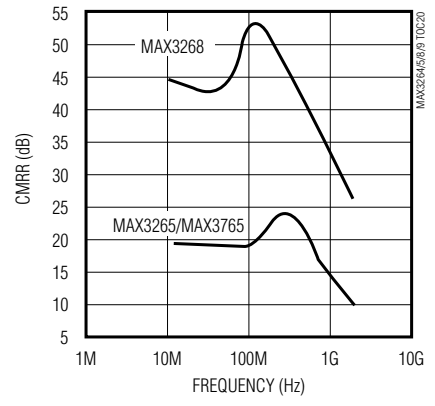
MAX3264 LOSS-OF-SIGNAL THRESHOLD vs. R_{TH}



MAX3265/MAX3765 LOSS-OF-SIGNAL THRESHOLD vs. R_{TH}



COMMON-MODE REJECTION RATIO vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
μMAX	TSSOP		
1, 4	3, 6	GND	Supply Ground
2	4	IN+	Noninverted Input Signal
3	5	IN-	Inverted Input Signal
5	8	TH	Loss-of-Signal Threshold. A resistor connected from this pin to ground sets the input signal level at which the loss-of-signal (LOS) output(s) will be asserted. Refer to *Typical Operating Characteristics* and *Design Procedure.*
6	9	$\overline{LOS}$	Inverted Loss-of-Signal Output. $\overline{LOS}$ is high when the level of the input signal is above the preset threshold set by the TH input. $\overline{LOS}$ is asserted low when the signal level drops below the threshold.
7, 10	11, 14	V_{CC}	Supply Voltage
8	12	OUT-	Inverted Data Output
9	13	OUT+	Noninverted Data Output
—	1	CAZ1	Offset-Correction-Loop Capacitor. A capacitor connected between this pin and CAZ2 extends the time constant of the offset correction loop.
—	2	CAZ2	Offset-Correction-Loop Capacitor. A capacitor connected between this pin and CAZ1 extends the time constant of the offset correction loop. Refer to *Design Procedure*.
—	7	LEVEL	Output Current Level. When this pin is not connected, the CML output current is approximately 16mA. When this pin is connected to ground, the output current increases to approximately 20mA. (In the MAX3265CUB/MAX3765CUB, LEVEL is internally connected to ground.)
—	10	LOS	Noninverted Loss-of-Signal Output. LOS is low when the level of the input signal is above the preset threshold set by the TH input. LOS asserts high when the signal level drops below the threshold.
—	15	SQUELCH	Squelch Input. The squelch function is disabled when SQUELCH is not connected or is set to a TTL-low level. When SQUELCH is set to a TTL-high level and LOS is asserted, the data outputs, OUT+, and OUT-, are forced to static levels. See sections *PECL Output Buffer* and *CML Output Buffer* for more information. (In the MAX3265/MAX3268/MAX3269 10-pin μMAX, SQUELCH is not connected. In the MAX3765, SQUELCH is internally connected to V_{CC}.)
—	16	N.C.	No Connection
EP	EP	Exposed Paddle	Ground. The exposed paddle must be soldered to the circuit–board ground for proper thermal performance.

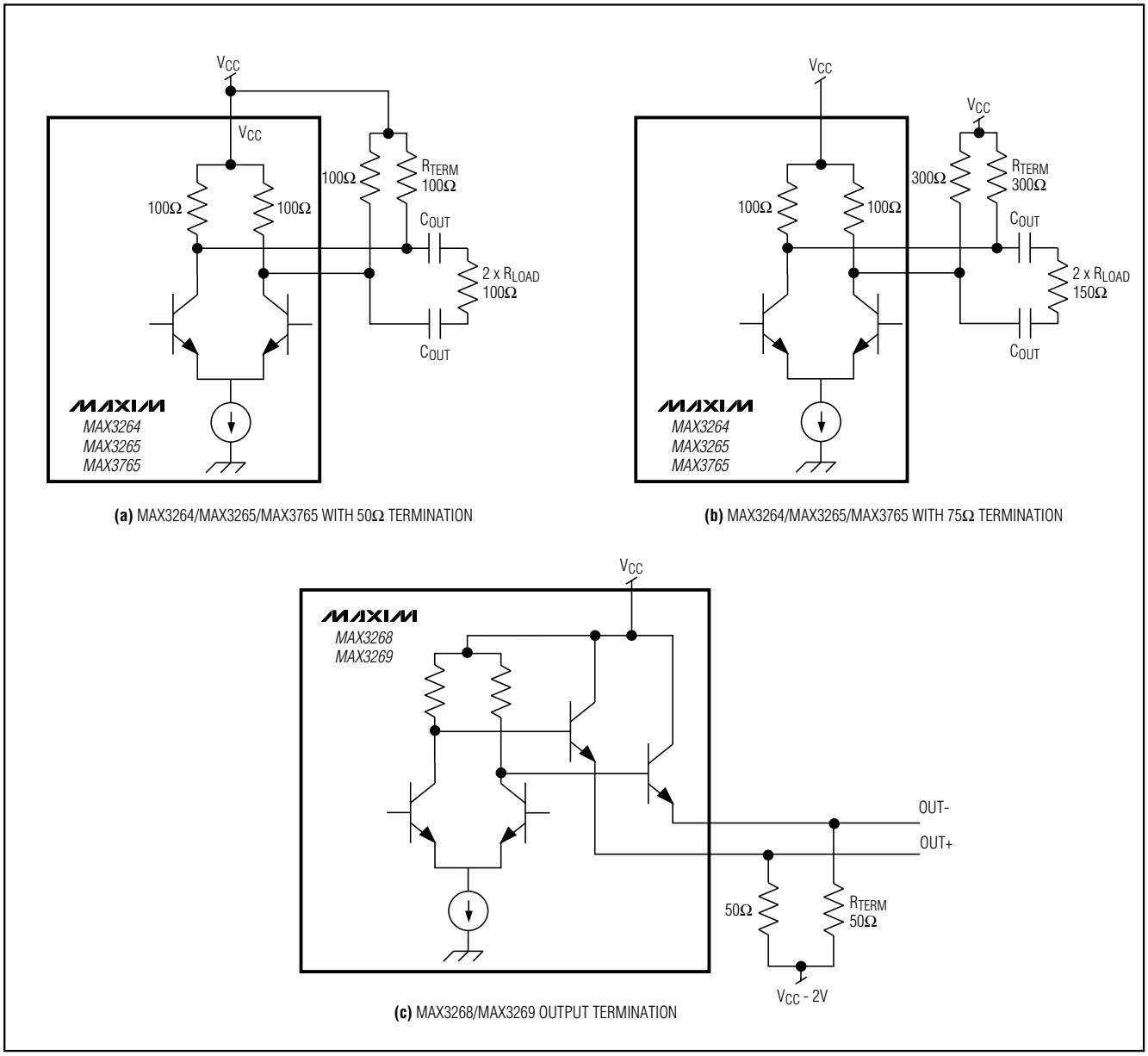
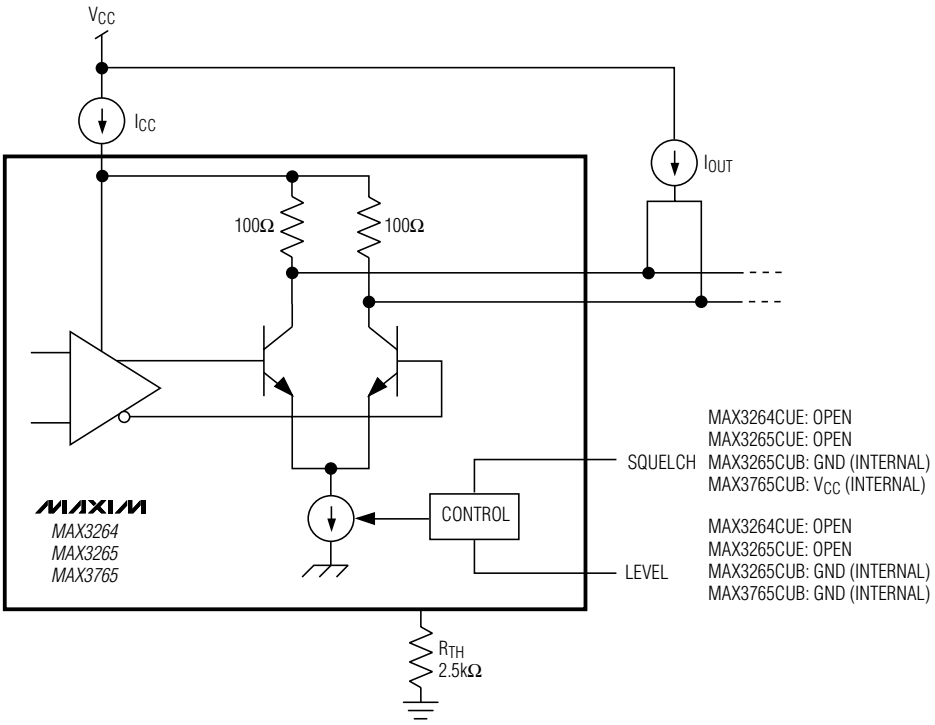
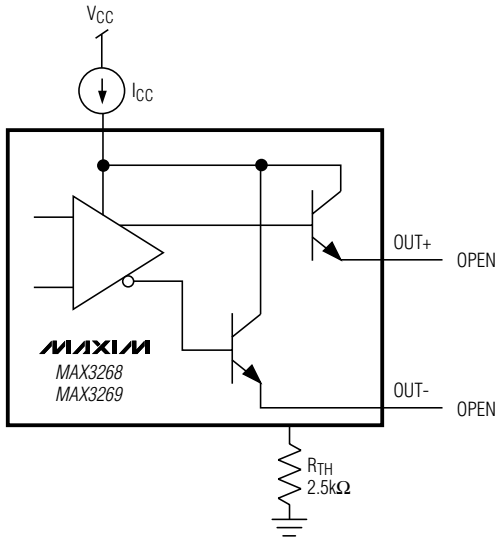


Figure 1. Data Output Termination



(a) CML SUPPLY CURRENT (I_{CC})



(b) PECL SUPPLY CURRENT (I_{CC})

Figure 2. Power-Supply Current Measurement

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

Detailed Description

Figure 3 is a functional diagram of the MAX3264/MAX3265/MAX3268/MAX3269/MAX3765 limiting amplifiers. A linear input buffer drives a multistage limiting amplifier and an RMS power detection circuit. Offset correction with lowpass filtering ensures low deterministic jitter. The output buffer produces a limited output signal. The MAX3264/MAX3265/MAX3765 produce a CML output, while the MAX3268/MAX3269 produce a PECL-compatible output signal. Schematics of these input/output circuits are shown in Figures 4 through 7.

RMS Power Detect with Loss-of-Signal Indicator

An RMS power detector looks at the signal from the input buffer and compares it to a threshold set by the TH resistor (see *Typical Operating Characteristics* for appropriate resistor values). The signal-detect information is provided to the LOS outputs, which are internally terminated with 8kΩ (MAX3265/MAX3269/MAX3765) or 16kΩ (MAX3264/MAX3268) pull-up resistors. The LOS outputs meet TTL voltage specifications when loaded with a resistor ≥ 4.7kΩ.

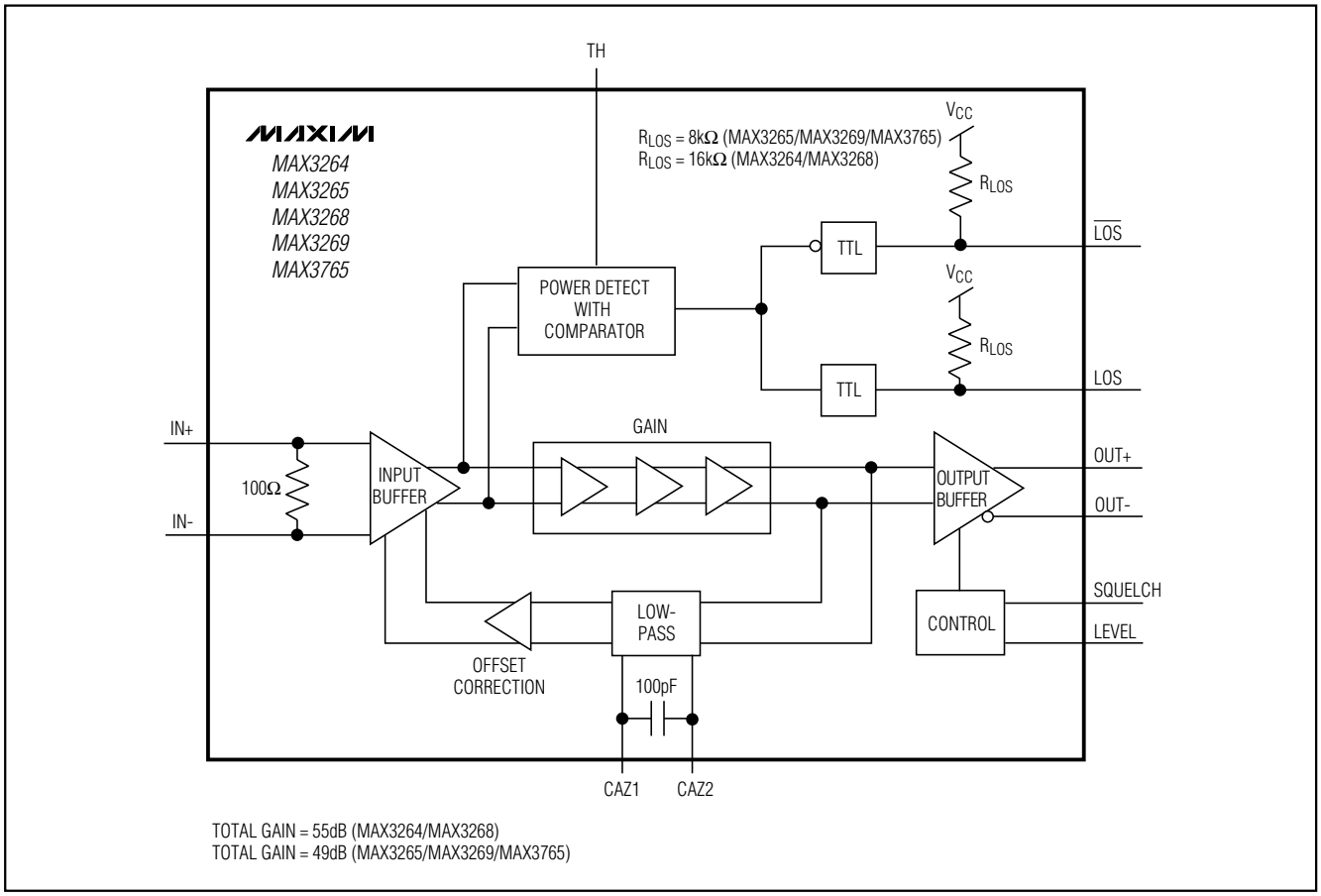


Figure 3. Functional Diagram

Input Buffer

The input buffer is designed to accept input signals from the MAX3266/MAX3267 transimpedance amplifiers. The input buffer provides a 100Ω input impedance between IN+ and IN-. Input VSWR is typically less than 2.0 for frequencies less than 2GHz. DC-coupling the inputs is not recommended; this prevents the DC offset-correction circuitry from functioning properly.

Gain Stage and Offset Correction

The limiting amplifier provides approximately 55dB (MAX3264/MAX3268) or 49dB (MAX3265/MAX3269/MAX3765) of gain. This large gain makes the amplifier susceptible to small DC offsets in the input signal. DC offsets as low as 1mV will reduce the accuracy of the power detection circuit and may cause deterministic jitter. A low-frequency feedback loop is integrated into the limiting amplifier to reduce input offset, typically to less than 100µV.

An external capacitor connected between CAZ1 and CAZ2, in parallel with internal capacitance, determines the time constant of the offset-correction circuit. The offset-correction circuit requires an average data-input mark density of 50% to prevent an increase in duty-cycle distortion and to ensure low deterministic jitter.

CML Output Buffer

The MAX3264/MAX3265/MAX3765 CML output circuits (Figure 7) provide high tolerance to impedance mismatches and inductive connectors. The output current can be set to two levels. When the LEVEL pin is left unconnected, output current is approximately 16mA. Connecting LEVEL to ground sets the output current to approximately 20mA.

The squelch function is enabled when the SQUELCH pin is set to a TTL-high level or connected to V_{CC}. The squelch function holds OUT+ and OUT- at a static voltage whenever the input signal power drops below the loss-of-signal threshold. In the 10-pin µMAX package of the MAX3265/MAX3268/MAX3269, the SQUELCH function is left internally unconnected. In the MAX3765, the SQUELCH function is always enabled by internally connecting it to V_{CC}. SQUELCH operation is described in Table 1.

Table 1. Squelch Operation

LEVEL PIN	VOLTAGE WHEN SQUELCHED	
	OUT-	OUT+
Open	V_{CC} - 100mV	V_{CC}
GND	V_{CC} - 100mV	V_{CC} - 100mV

Internal Input/Output Schematics

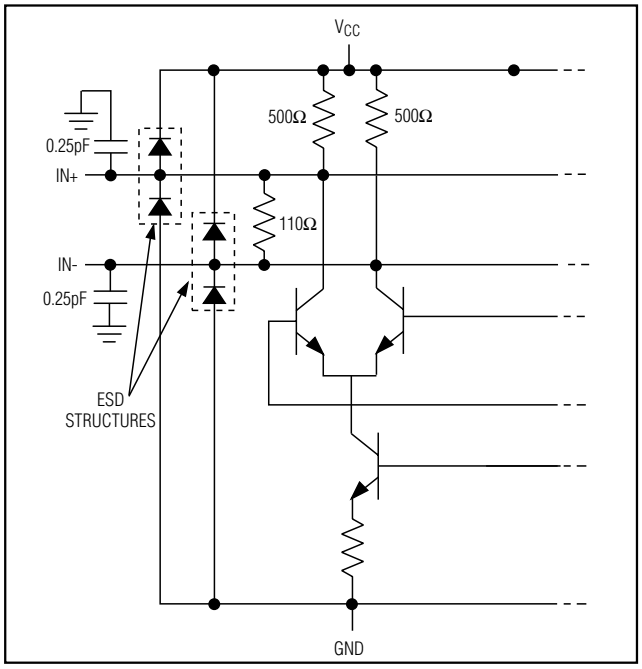


Figure 4. Input Circuit

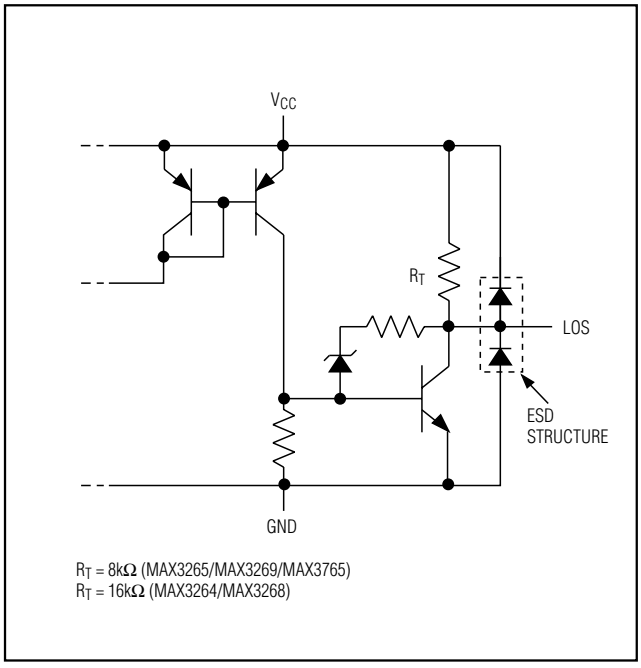


Figure 5. LOS Output Circuit

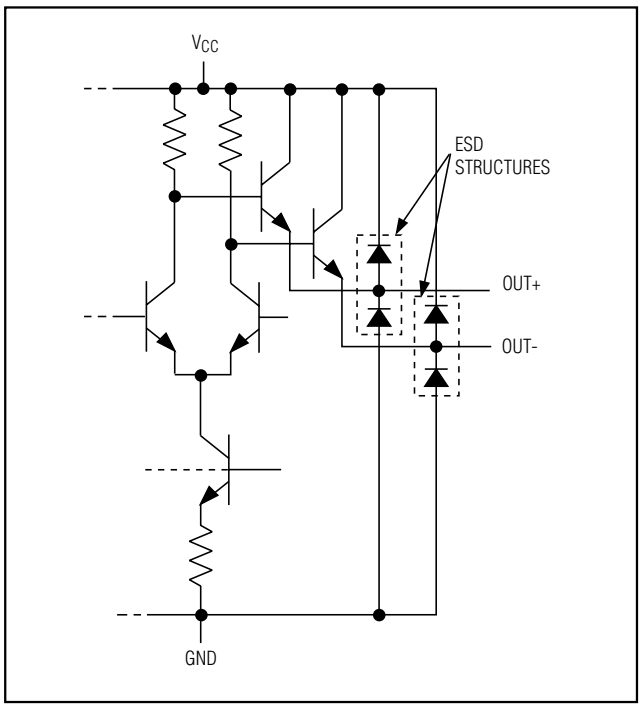


Figure 6. PECL Output Circuit

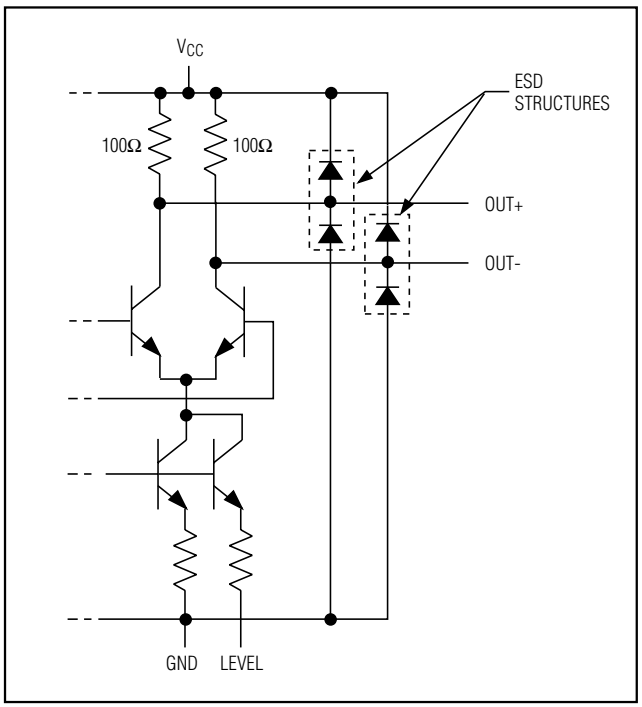


Figure 7. CML Output Circuit

The buffer's output impedance is determined by the parallel combination of internal and external pull-up resistors, which are chosen to match the impedance of the transmission line (Figure 1). The output buffer can be AC- or DC-coupled to the load.

PECL Output Buffer

The MAX3268/MAX3269 offer an industry-standard PECL output. The PECL outputs should be terminated to V_{CC} - 2V. Figure 6 shows the PECL output circuit. The squelch function forces OUT+ to a high level and OUT- to a low level when the input is below the programmed LOS threshold. In the 10-pin µMAX, SQUELCH is left unconnected.

Design Procedure

Program the LOS Assert Threshold

The loss-of-signal threshold is programmed by external resistor R_{TH}. See the LOS Threshold vs. R_{TH} graph in the *Typical Operating Characteristics.*

Select the Coupling Capacitors

The coupling capacitors (C_{IN}, C_{OUT}) should be selected to minimize the receiver's deterministic jitter. Jitter is minimized when the input low-frequency cutoff (f_{IN}) is placed at a low frequency.

$$f_{IN} = 1 / [2\pi(50)(C)]$$

For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, select (C_{IN}, C_{OUT}) ≥ 0.01µF, which provides f_{IN} < 320kHz. For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN}, C_{OUT}) ≥ 0.1µF, which provides f_{IN} < 32kHz.

Select the Offset-Correction Capacitor (MAX3264/MAX3265 TSSOP only)

To maintain stability, it is important to keep a one-decade separation between f_{IN} and the low-frequency cutoff (f_{OC}) associated with the DC-offset-correction circuit.

$$f_{OC} = 75 / [2\pi\ 60k\ (C_{AZ} + 100pF)]$$

$$= 200 \times 10^{-6} / (C_{AZ} + 100pF)$$

For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, leave pins CAZ1, and CAZ2 open (f_{OC} = 2MHz). For ATM/SONET or other applications using scrambled NRZ data, select C_{AZ} ≥ 0.1µF, which typically provides f_{OC} = 2kHz.

Applications Information

Optical Hysteresis

In an optical receiver, the electrical power change at the limiting amplifier is 2x the optical power change.

As an example, if a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage input to the limiting amplifier also increases by a factor of two.

The optical power change is 10log(2x / x) = 10log(2) = +3dB.

At the limiting amplifier, the electrical power change is:

$$10\log\frac{(2V_{IN})^2 / R_{IN}}{V_{IN}^2 / R_{IN}} = 10\log(2^2) = 20\log(2) = +6dB$$

The MAX3264/MAX3265/MAX3268/MAX3269/MAX3765's typical voltage hysteresis is 4.4dB. This provides an optical hysteresis of 2.2dB.

GBIC Loss of Signal

In a GBIC application, the GBIC's LOS output must be high impedance when V_{CC}_MODULE = GND. Figure 8 shows the recommended circuit to maintain high impedance. ESD protection diodes on the MAX3264/MAX3265/MAX3268/MAX3269/MAX3765 LOS outputs can be turned on when V_{CC}_HOST > V_{CC}_MODULE.

PECL Terminations

The standard PECL termination (50Ω to V_{CC} - 2V) is recommended for best performance and output characteristics (see Figure1). The data outputs operate at high speed and should always drive transmission lines with matched, balanced terminations.

Figure 9 shows an alternate method for terminating the data outputs. The technique provides approximately 8mA DC bias current, with a 45Ω AC load, for the output termination. This technique is useful for viewing the output on an oscilloscope or changing the PECL reference voltage.

Wire Bonding Dice

For high current density and reliable operation, the MAX3264/MAX3265/MAX3268/MAX3269 use gold metalization. Make connections to the dice with gold wire only, and use ballbonding techniques (wedge bonding is not recommended). Die-pad size is 4mils square, with a 6mil pitch. Die thickness is 15mils (0.375mm).

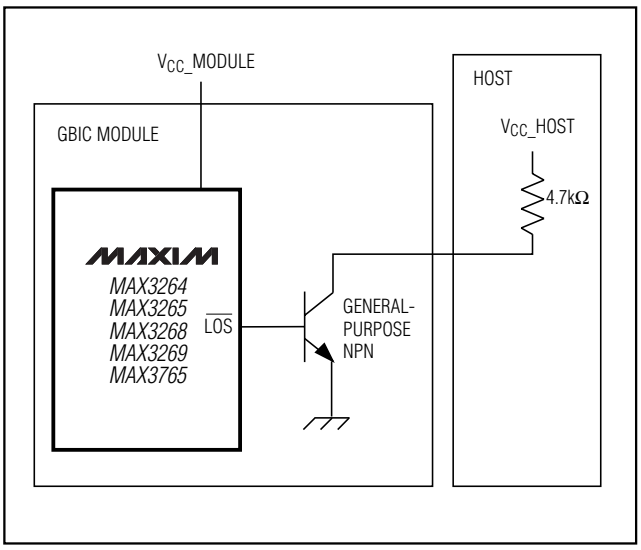


Figure 8. Recommended GBIC LOS Circuit

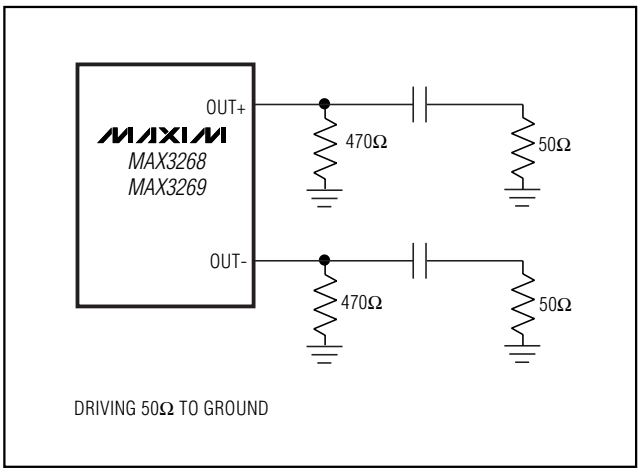
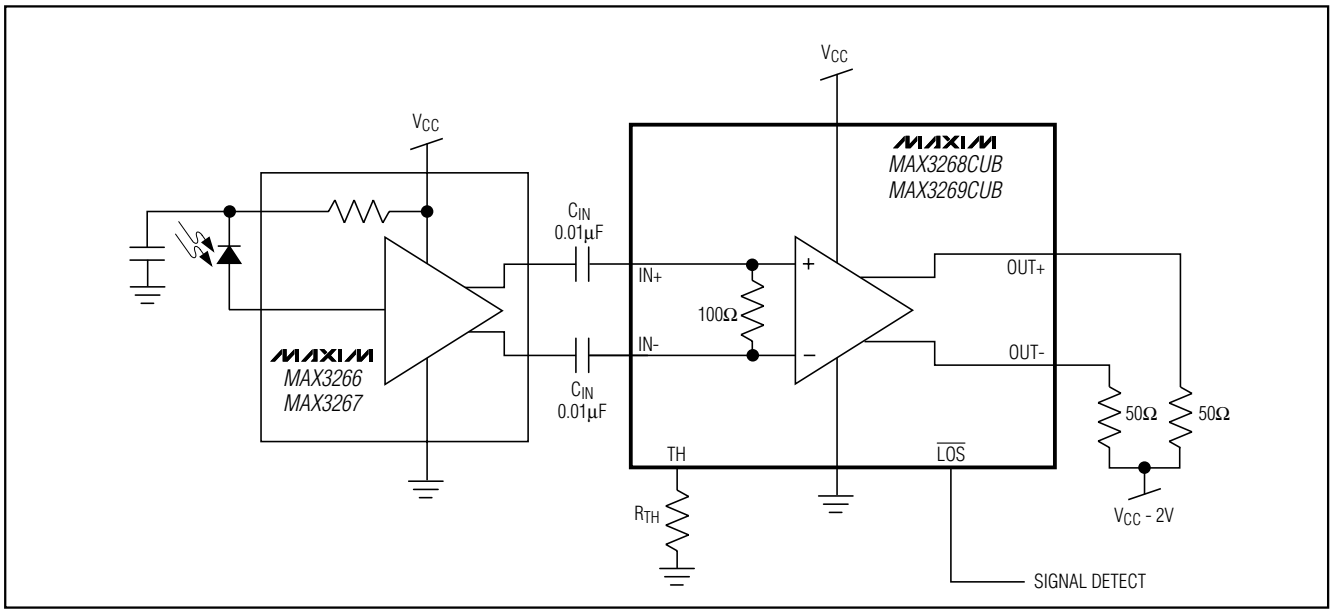


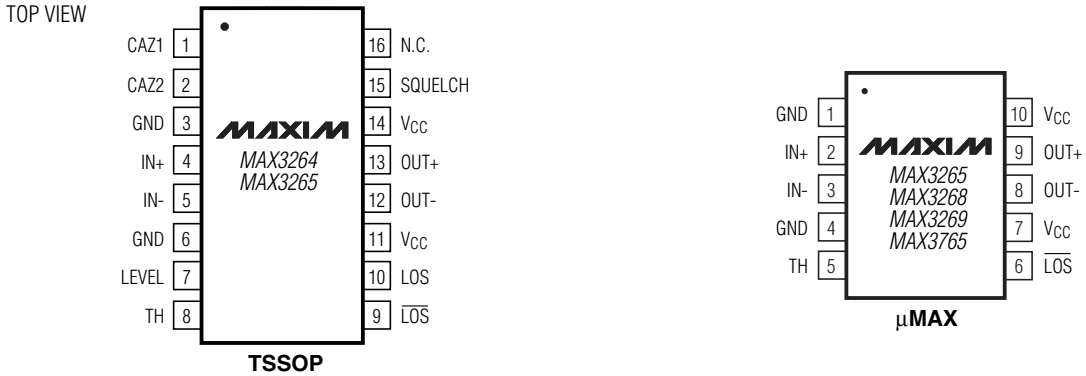
Figure 9. Alternative PECL Termination

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

Typical Operating Circuits (continued)



Pin Configurations



NOTE: EXPOSED PADDLE IS GROUND.

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

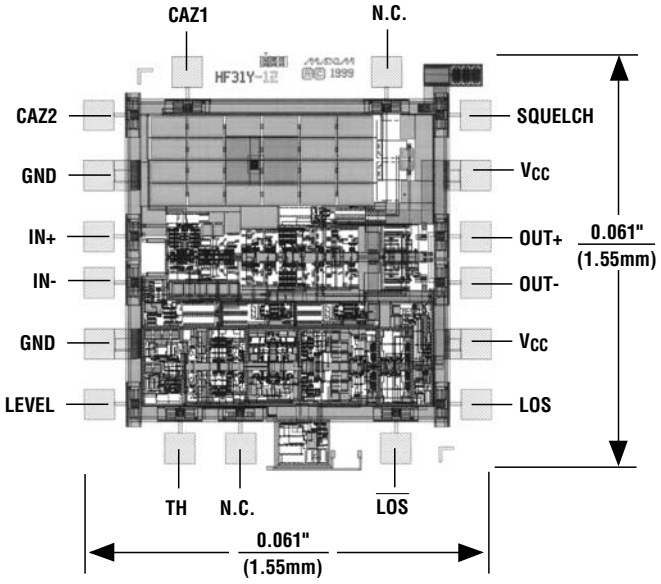
Selector Guide

PART	OUTPUT	DATA RATE (Gbps)	PIN-PACKAGE	SQUELCH FUNCTION	CML OUTPUT LEVEL
MAX3264	CML	1.25	16 TSSOP-EP	Selectable	Selectable
MAX3265	CML	2.5	16 TSSOP-EP	Selectable	Selectable
			10 µMAX-EP	Disabled	Maximum*
MAX3268	PECL	1.25	10 µMAX-EP	Disabled	N/A
MAX3269	PECL	2.5	10 µMAX-EP	Disabled	N/A
MAX3765	CML	2.5	10 µMAX-EP	Enabled	Maximum*

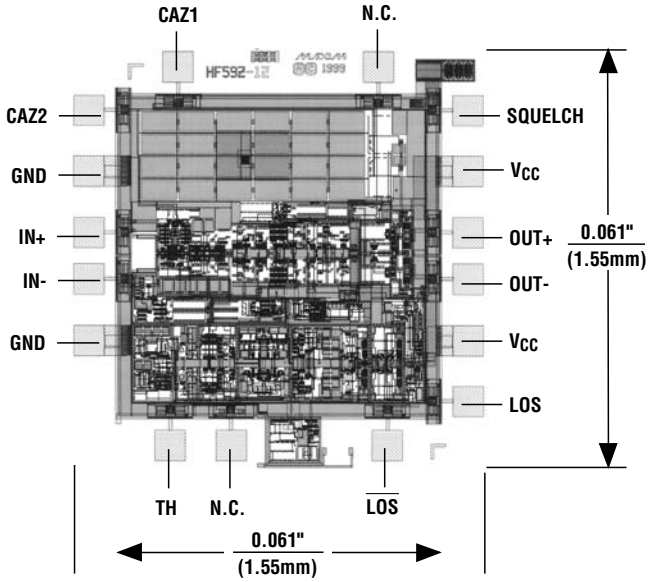
**LEVEL pin grounded*

Chip Topographies

MAX3264/MAX3265/MAX3765



MAX3268/MAX3269



MAX3264/MAX3265/MAX3765
TRANSISTOR COUNT: 726

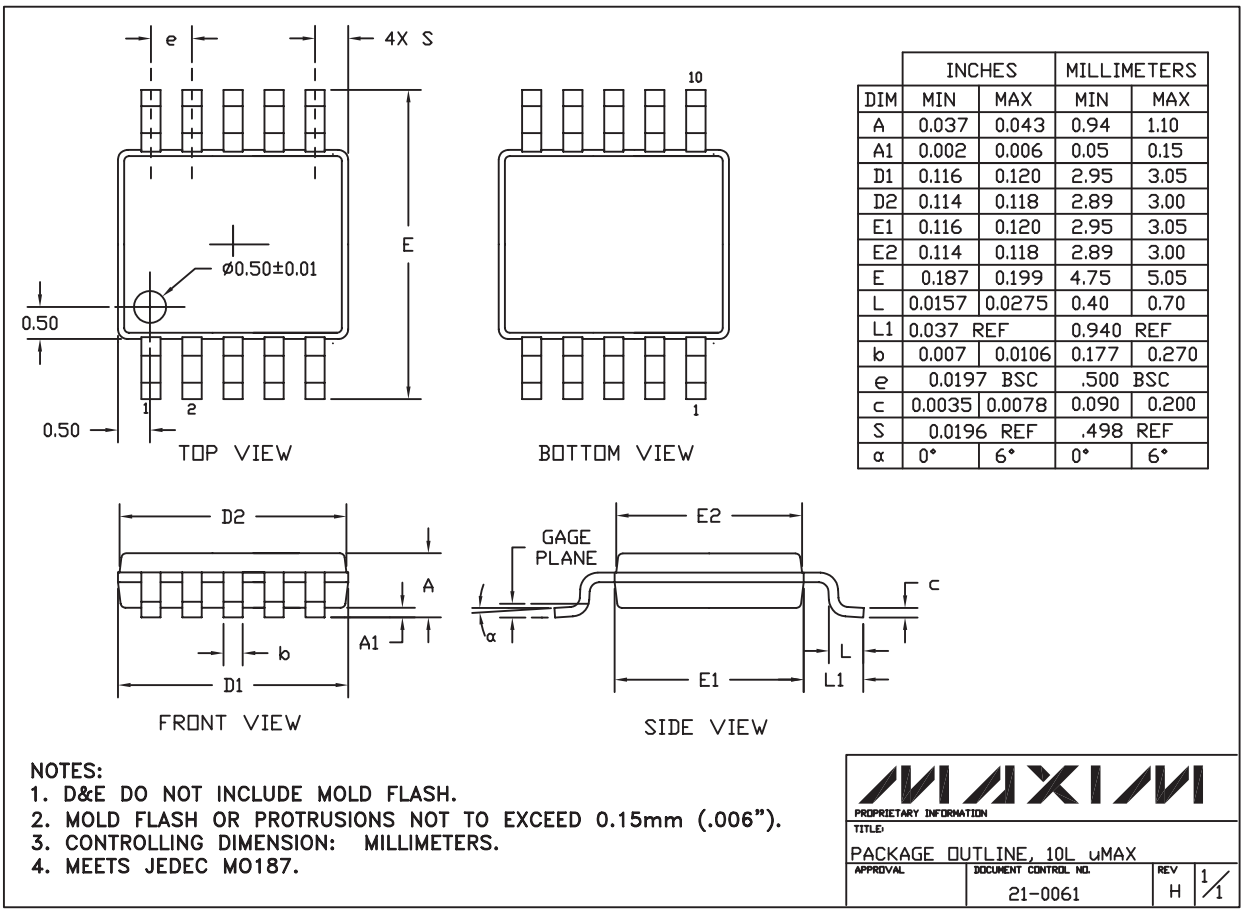
MAX3268/MAX3269 TRANSISTOR COUNT: 728

SUBSTRATE CONNECTED TO GND

3.0V to 5.5V, 1.25Gbps/2.5Gbps Limiting Amplifiers

Package Information

10LUMAX.EPS

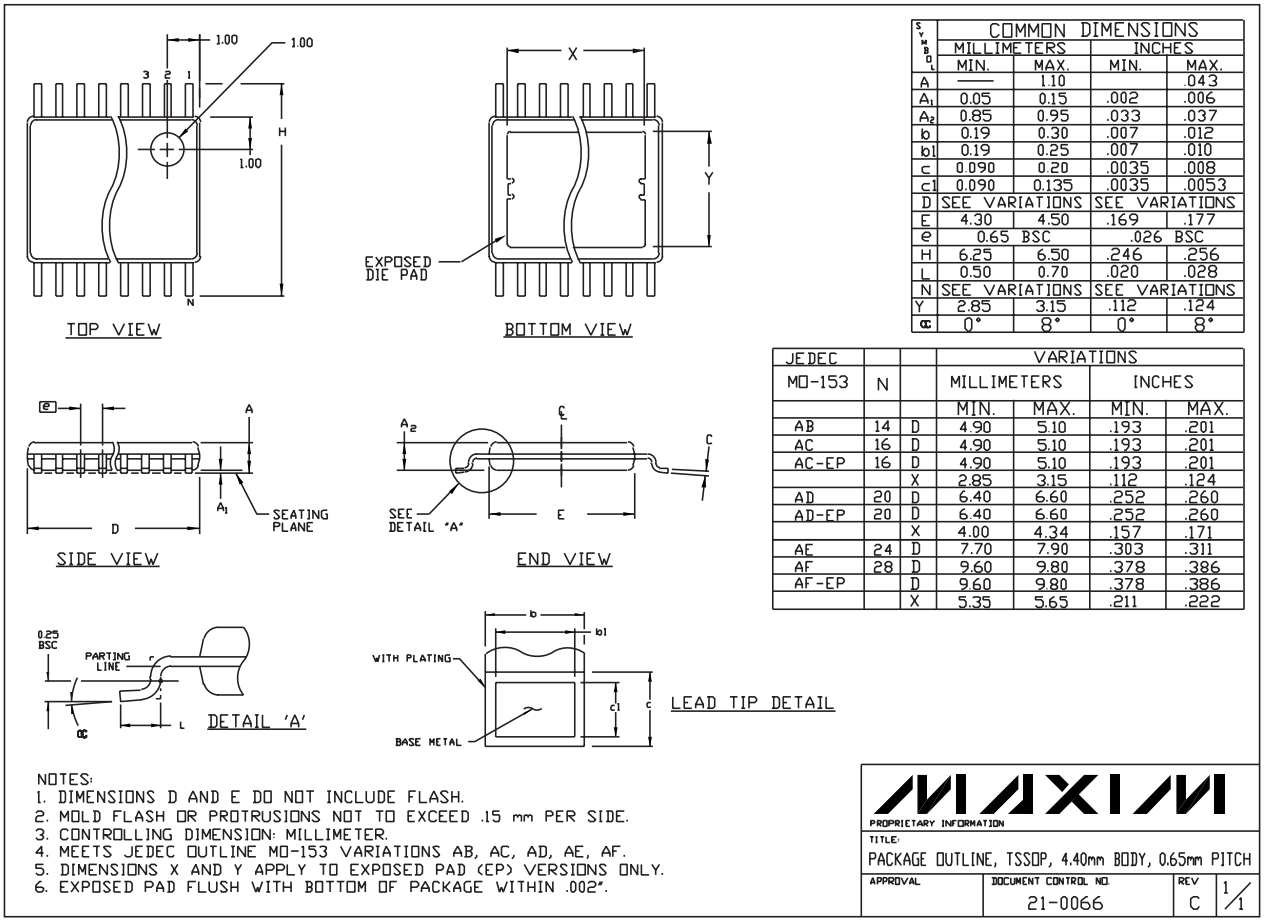


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10
A1	0.002	0.006	0.05	0.15
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
E	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO187.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0061 | REV H | 1/1

Package Information



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	C	1/1

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